CLAIMS:

1. A method of forming a dynamic random access memory (DRAM) comprising:

forming an insulative layer over a substrate having a plurality of conductive lines which extend within a memory array area and a peripheral area outward of the memory array; and

contemporaneously etching capacitor container openings over the memory array and contact openings within the insulative layer over conductive line portions within the peripheral area.

2. The method of claim 1, wherein the etching of the capacitor container openings and contact openings comprises etching said openings to have substantially the same opening dimensions.

3. The method of claim 1, wherein the etching of the capacitor container openings and contact openings comprises exposing insulative cap portions of conductive lines in the peripheral area.

4. The method of claim 1, wherein the etching of the capacitor container openings and contact openings comprises exposing insulative cap portions of conductive lines in both the memory array area and the peripheral area.

5. The method of claim 1, wherein the etching of the capacitor container openings and contact openings comprises:

etching said openings to have substantially the same opening dimensions; and

exposing insulative cap portions of conductive lines in the peripheral area.

6. The method of claim 1 further comprising after the etching, contemporaneously forming conductive material within the capacitor container openings and contact openings, the conductive material within the capacitor container openings comprising at least a portion of a capacitor electrode layer.

7. The method of claim 1 further comprising patterning and removing conductive cell plate material within the memory array, said removing also removing conductive material from within said contact openings over said conductive line portions.

8. The method of claim 1 further comprising after the etching:

contemporaneously forming conductive material within the capacitor container openings and contact openings, the conductive material within the capacitor container openings comprising at least a portion of a capacitor electrode layer; and

removing the conductive material from within the contact openings within the peripheral area and removing portions of an overlying insulative cap from over the conductive line portions to expose conductive material of the conductive lines within the peripheral area.

9. The method of claim 1 further comprising after the etching:

contemporaneously forming conductive material over the substrate and within the capacitor container openings and contact openings, the conductive material within the capacitor container openings comprising at least a portion of a capacitor electrode layer;

removing the conductive material from within the contact openings within the peripheral area and removing portions of an overlying insulative cap from over the conductive line portions to expose conductive material of the conductive lines within the peripheral area; and

after the removing, forming additional conductive material over and in electrical communication with the conductive line portions.

10. A method of forming a dynamic random access memory (DRAM) comprising:

forming an insulative layer over a substrate having a plurality of conductive lines which extend within a memory array area and a peripheral area outward of the memory array; and

in a common photomasking step, etching capacitor container openings over the memory array and contact openings over conductive line portions within the peripheral area.

11. The method of claim 10, wherein the etching of the capacitor container openings and the contact openings comprises contemporaneously etching at least portions of the openings.

12. A method of forming a dynamic random access memory (DRAM) comprising:

forming a patterned masking layer over a substrate having a plurality of openings formed within an insulative layer, some of the openings comprising capacitor container openings within a memory array and having at least a portion of a capacitor electrode layer disposed therein, other of the openings comprising conductive line contact openings disposed over conductive lines within a peripheral area outward of the memory array; and

with said common patterned masking layer, removing unmasked portions of the capacitor electrode layer within the memory array, and removing material from over portions of the conductive lines within the peripheral area sufficient to expose conductive material of the conductive line portions.

13. The method of claim 12, wherein the removing of the material from over portions of the conductive lines within the peripheral area comprises removing conductive material from which the capacitor electrode layer was formed.

14. The method of claim 12, wherein the removing of the material from over portions of the conductive lines within the peripheral area comprises removing insulative cap portions from over the conductive line portions.

15. The method of claim 12, wherein the removing of the material from over portions of the conductive lines within the peripheral area comprises removing insulative cap portions comprising a nitride material from over the conductive line portions.

16. The method of claim 12, wherein the removing of the unmasked portions of the capacitor electrode layer and the removing of the material from over portions of the conductive lines within the peripheral area comprises contemporaneously removing conductive material from within the memory array and from within the contact openings within the peripheral area.

17. The method of claim 12, wherein the removing of the material from over portions of the conductive lines within the peripheral area comprises removing first and second conductive materials from over the conductive line portions.

18. The method of claim 12, wherein the removing of the material from over portions of the conductive lines within the peripheral area comprises removing first and second conductive materials from over the conductive line portions, the first and second conductive materials being elevationally spaced apart and separated by an intervening dielectric region.

19. A method of forming a dynamic random access memory (DRAM) comprising:

forming a plurality of conductive lines over a substrate having a memory array area and a peripheral area outward of the memory array area, the conductive lines having an insulative material layer formed thereover;

forming a storage capacitor electrode layer over the substrate; and

using a common etch chemistry, removing material of the insulative material layer and material of the storage capacitor electrode layer within the peripheral area.

20. The method of claim 19, wherein no material of the storage capacitor electrode layer within the memory array area is removed during said removing.

21. The method of claim 19, wherein the insulative material comprises individual insulative material caps over the conductive lines.

22. The method of claim 19, wherein:

the insulative material comprises individual insulative material caps over the conductive lines; and

the removing of the material of the insulative material layer comprises removing insulative material cap portions from over conductive lines in the peripheral area.

23. The method of claim 19, wherein the insulative material layer comprises a first insulative material layer and further comprising prior to the forming of the storage capacitor electrode layer, contemporaneously forming openings within a second insulative material layer over the conductive lines within the peripheral area and the memory array area, the openings over the peripheral area as initially formed exposing the first insulative material layer but not conductive material of the conductive lines.

24. The method of claim 19, wherein the insulative material layer comprises first insulative material layer caps over the conductive lines, and further comprising prior to the forming of the storage capacitor electrode layer, contemporaneously forming openings within a second insulative material layer over the conductive lines within the peripheral area and the memory array area, the openings over the peripheral area as initially formed exposing the first insulative material layer but not conductive material of the conductive lines.

25. The method of claim 19, wherein the insulative material comprises silicon nitride and the capacitor electrode layer comprises a conductively doped silicon.

26. A method of forming a dynamic random access memory (DRAM) comprising:

forming a plurality of conductive lines over a substrate having a memory array area and a peripheral area outward of the memory array area, the conductive lines having an insulative material layer formed thereover;

forming a storage capacitor storage node electrode layer over the memory array and the peripheral area; and

contemporaneously removing material of the insulative material layer and material of the storage capacitor storage node electrode layer within the peripheral area.

27. A method of forming a dynamic random access memory (DRAM) comprising:

forming a plurality of conductive plugs received over substrate node locations over which storage capacitors are to be formed within a memory array area; and

after the forming of the plugs, removing insulative material over and exposing conductive material of conductive lines which are formed within a peripheral area outward of the memory array area, said exposing being a first-in-time exposure of conductive material of the conductive lines in the peripheral area after provision of said insulative material thereover.

28. The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material, forming capacitor container openings within a second insulative material over conductive lines within the memory array area.

29. The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material, contemporaneously forming both capacitor container openings within a second insulative material over conductive lines within the memory array area, and contact openings within the second insulative material over the conductive lines within the peripheral area.

30. The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material:

contemporaneously forming both capacitor container openings within a second insulative material over conductive lines within the memory array area, and contact openings within the second insulative material over the conductive lines within the peripheral area; and

forming a capacitor electrode layer within the capacitor container openings and the contact openings.

31. The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material:

contemporaneously forming both capacitor container openings within a second insulative material over conductive lines within the memory array area, and contact openings within the second insulative material over the conductive lines within the peripheral area; and

forming a pair of capacitor electrode layers and an intervening dielectric region therebetween within the capacitor container openings and the contact openings.

32. The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material:

contemporaneously forming both capacitor container openings within a second insulative material over conductive lines within the memory array area, and contact openings within the second insulative material over the conductive lines within the peripheral area;

forming a capacitor electrode layer within the capacitor container openings and the contact openings; and

removing the capacitor electrode layer from within the contact openings and not from within the capacitor container openings.

33. The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material:

contemporaneously forming both capacitor container openings within a second insulative material over conductive lines within the memory array area, and contact openings within the second insulative material over the conductive lines within the peripheral area;

forming a capacitor electrode layer within the capacitor container openings; and

wherein the removing of the first insulative material comprises using an etch chemistry effective to remove both the first insulative material and selected portions of the capacitor electrode layer over the memory array.

34. The method of claim 27, wherein the forming of the plurality of conductive plugs comprises forming conductive material over the insulative material over the conductive lines within the peripheral area.

35. The method of claim 27, wherein the insulative material comprises a first insulative material, and wherein:

the forming of the plurality of conductive plugs comprises forming conductive material over the first insulative material over the conductive lines within the peripheral area, and further comprising prior to the removing of the first insulative material, forming capacitor container openings over and exposing conductive plug portions within the memory array.

36. The method of claim 27, wherein the insulative material comprises a first insulative material, and wherein:

the forming of the plurality of conductive plugs comprises forming conductive material over the first insulative material over the conductive lines within the peripheral area, and further comprising prior to the removing of the first insulative material, forming both capacitor container openings over and exposing conductive plug portions within the memory array, and contact openings over conductive lines within the peripheral area and exposing conductive material portions over the first insulative material.

37. The method of claim 27, wherein the insulative material comprises a first insulative material, and wherein:

the forming of the plurality of conductive plugs comprises forming conductive material over the first insulative material over the conductive lines within the peripheral area, and further comprising prior to the removing of the first insulative material, forming both capacitor container openings over and exposing conductive plug portions within the memory array, and contact openings over conductive lines within the peripheral area and exposing conductive material portions over the first insulative material; and

forming a capacitor electrode layer within the capacitor container openings and the contact openings.

38. The method of claim 27, wherein the insulative material comprises a first insulative material, and wherein:

the forming of the plurality of conductive plugs comprises forming conductive material over the first insulative material over the conductive lines within the peripheral area, and further comprising prior to the removing of the first insulative material, forming capacitor container openings over and exposing conductive plug portions within the memory array; and

wherein the removing of the first insulative material comprises using an etch chemistry effective to remove both conductive material portions over the first insulative material and the first insulative material.

39. A method of forming a dynamic random access memory (DRAM) comprising:

forming a plurality of conductive plugs received over substrate node locations over which storage capacitors are to be formed within a memory array area; and

after the forming of the plugs, removing substantial portions of individual conductive line insulative caps over and exposing conductive material of conductive lines which are formed within a peripheral area outward of the memory array area.

40. The method of claim 39 further comprising after the forming of the plurality of conductive plugs:

forming an insulative material layer over the substrate; and

forming a plurality of openings received within the insulative material layer, some of the openings comprising capacitor container openings within which storage capacitors are to be formed, other of the openings comprising first contact openings formed over the insulative caps of the conductive lines within the peripheral area.

41. The method of claim 39 further comprising after the forming of the plurality of conductive plugs:

forming an insulative material layer over the substrate;

forming a plurality of openings received within the insulative material layer, some of the openings comprising capacitor container openings within which storage capacitors are to be formed, other of the openings comprising first contact openings formed over the insulative caps of the conductive lines within the peripheral area; and

forming a capacitor electrode layer within the capacitor container openings and the first contact openings.

42. The method of claim 39 further comprising after the forming of the plurality of conductive plugs:

forming an insulative material layer over the substrate;

forming a plurality of openings received within the insulative material layer, some of the openings comprising capacitor container openings within which storage capacitors are to be formed, other of the openings comprising first contact openings formed over the insulative caps of the conductive lines within the peripheral area;

forming a pair of capacitor electrode layers within the capacitor container openings and the first contact openings;

forming a patterned masking layer over the capacitor container openings; and

removing unmasked portions of the pair of capacitor electrode layers.

43. The method of claim 39 further comprising after the forming of the plurality of conductive plugs:

forming an insulative material layer over the substrate;

forming a plurality of openings received within the insulative material layer, some of the openings comprising capacitor container openings within which storage capacitors are to be formed, other of the openings comprising first contact openings formed over the insulative caps of the conductive lines within the peripheral area;

forming a pair of capacitor electrode layers within the capacitor container openings and the first contact openings;

forming a patterned masking layer over the capacitor container openings; and

removing unmasked portions of the pair of capacitor electrode layers, and wherein the removing of the substantial portions of the individual conductive line insulative caps comprises removing said portions with the patterned masking layer in place.

44. A method of forming a dynamic random access memory (DRAM) comprising:

forming a plurality of conductive lines over a substrate having a memory array area and a peripheral area outward of the memory array area;

forming conductive material over the substrate comprising:

conductive plugs received over substrate node locations over which storage capacitors are to be formed within the memory array area, and

conductive material received over portions of some of the conductive lines within the peripheral area;

forming openings through an insulative material and exposing the conductive plugs within the memory array area and the conductive material within the peripheral area;

forming a storage capacitor electrode layer within the openings; and

removing portions of the storage capacitor electrode layer within the memory array area and peripheral area sufficient to form a storage capacitor electrode within the memory array and entirely remove the storage capacitor electrode layer from within the peripheral area and outwardly expose conductive portions of conductive lines within the peripheral area.

45. The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a cell plate layer within the openings.

46. The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a cell plate layer within the openings, and wherein the removing of the storage capacitor electrode layer comprises doing so in a common masking step.

47. The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a cell plate layer within the openings, and wherein the removing of the storage capacitor electrode layer comprises doing so in a common etching step.

48. The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a storage node layer within the openings.

49. The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a storage node layer within the openings, and wherein the removing of the storage capacitor electrode layer comprises doing so in multiple removing steps.